21. (Original) The device of claim 20, further comprising a selection signal generator for selecting a refresh operation between the first refresh operation and the second refresh operation.

22. (Original) The device of claim 21, wherein the selection signal generator generating a selecting signal.

23. (Original) The device of claim 22, wherein the selection signal is generated by programming means.

24. (Original) The device of claim 23, wherein the programming means is a mode register set command.

25. (Original) The device of claim 22, wherein the selection signal is input from an external pin.

26. (Original) The device of claim 22, wherein the selection signal is a fuse information signal.

27. (Original) An integrated circuit memory device, comprising:

a delay locked loop (DLL) circuit, the DLL circuit generates a first clock signal based on a reference clock signal and locking information, the locking information being